DATA SHEET

TSA5055T
2.65 GHz bidirectional I²C-bus controlled synthesizer

Product specification
1999 Aug 11
Supersedes data of November 1991
File under Integrated Circuits, IC02

Philips
Semiconductors

PHILIPS

2.65 GHz bidirectional I²C-bus controlled synthesizer

TSA5055T

FEATURES

- Complete 2.65 GHz single-chip system
- Low power 5 V, 60 mA
- I²C-bus programming
- In-lock flag
- Varicap drive disable
- Low radiation
- 5-level Analog to Digital Converter (ADC)
- Address selection for Picture-In-Picture (PIP), DBS tuner, etc.
- 6 controllable outputs, 4 bidirectional
- Power-down flag
- Available in SOT109-1 (SO16) package
- Symmetrical or asymmetrical drive.

APPLICATIONS

- Satellite TV
- High IF cable tuning systems.

GENERAL DESCRIPTION

The TSA5055T is a single-chip PLL frequency synthesizer designed for satellite TV tuning systems. It may be used with a symmetrical input (pins 13 and 14) or with an asymmetrical input (pin 13).

Control data is entered via the I²C-bus; five serial bytes are required to address the device, select the oscillator frequency, program the six output ports and set the charge-pump current. Four of these ports can also be used as input ports (three general purpose I/O ports, one ADC). Digital information concerning these ports can be read out of the TSA5055T on the SDA line (one status byte) during a READ operation. A flag is set when the loop is 'in-lock' and is read during a READ operation. The device has one fixed I²C-bus address and three programmable addresses, programmed by applying a specific voltage to port 3. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	4.5	5	5.5	V
I_{CC}	supply current	–	60	80	mA
f_{RF}	RF input frequency range	1	–	2.65	GHz
$V_{I\ (rms)}$	input voltage level (RMS value)				
	1 to 1.8 GHz	50	–	300	mV
	1.8 to 2.65 GHz	70	–	300	mV
f_{XTAL}	crystal oscillator frequency	3.2	4	4.48	MHz
z_{XTAL}	crystal oscillator impedance (absolute value)	600	1000	–	Ω
I_O	open-collector output current P7, P6, P5 and P4	–	–	10	mA
	output current P3 and P0	–	1	–	mA
T_{amb}	ambient temperature	–20	–	+85	°C
T_{stg}	storage temperature	–40	–	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	CODE
TSA5055T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

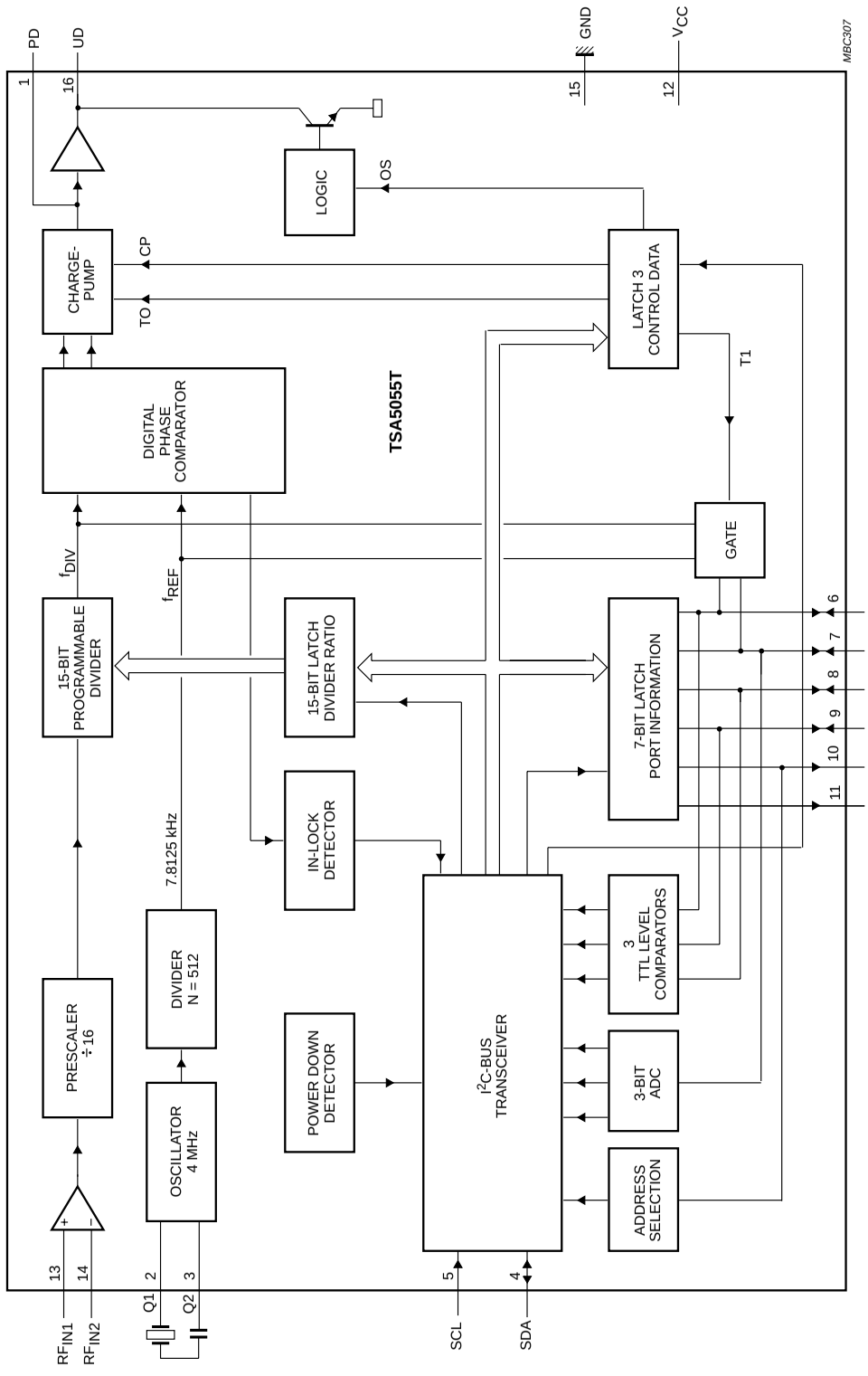


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
PD	1	charge-pump output
Q1	2	crystal oscillator input 1
Q2	3	crystal oscillator input 2
SDA	4	serial data input/output
SCL	5	serial clock input
P7	6	port output/input (general purpose)
P6	7	port output/input (ADC)
P5	8	port output/input (general purpose)
P4	9	port output/input (general purpose)
P3	10	port output (also used for address selection)
P0	11	port output
V_{CC}	12	voltage supply
RF_{IN1}	13	RF signal input 1
RF_{IN2}	14	RF signal input 2 (decoupled)
GND	15	ground
UD	16	drive output

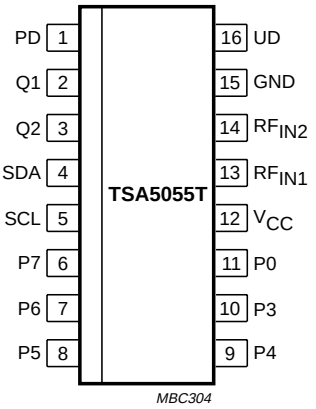


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The TSA5055T is controlled via the 2-wire I²C-bus. For programming, there is one (7-bit) module address and the R/$\overline{W}$ bit for selecting READ or WRITE mode.

WRITE mode: R/$\overline{W}$ = 0; see Table 1

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are needed to fully program the TSA5055T. The bus transceiver has an auto-increment facility that permits the programming of the TSA5055T within one single transmission (address + four data bytes).

The TSA5055T can also be partly programmed on the condition that the first data byte following the address is byte 2 or byte 4.

The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge-pump and port information (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning. At power-on, the ports are set to the high-impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of the RF signal is first divided by 16, the step size is 125 kHz. A 3.2 MHz crystal can offer a step size of 100 kHz.

Table 1 Write data format; see notes 1 to 13

BYTE	MSB			DATA BYTE				LSB	COMMAND	
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	1	1	1	OS	A	byte 4
Output ports, control bits	P7	P6	P5	P4	P3	X	X	P0	A	byte 5

Notes

1. MA1 and MA0: programmable address bits (see Table 3).
2. A: Acknowledge bit.
3. N14 to N0: programmable divider bits.
4. $N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2^{1} + N0$.
5. CP: charge-pump current. CP = 0: 50 μA; CP = 1: 220 μA.
6. P7 to P4 = 1: open-collector outputs are active.
7. P7 to P3 and P0 = 0: outputs are in high-impedance state.
8. P3 and P0 = 1: current-limited outputs are active.
9. T1, T0 and OS = 0, 0 and 0: normal operation.
10. T1 = 1: P6 = f_{REF} and P7 = f_{DIV}.
11. T0 = 1: 3-state charge-pump.
12. OS = 1: Operational amplifier output is switched off (varicap drive disable).
13. X: don't care.

READ mode: R/$\overline{W}$ = 1; see Table 2

Data can be read out of the TSA5055T by setting the R/$\overline{W}$ bit to 1. After the slave address has been recognized, the TSA5055T generates an Acknowledge signal (A) and the first data byte (status byte) is transferred to the SDA line (MSB first). Data is valid on the SDA line while the SCL clock signal is HIGH.

A second data byte can be read out of the TSA5055T if the processor generates an Acknowledge signal on the SDA line. End of transmission will occur if the processor does not send an Acknowledge signal.

The TSA5055T will then release the data line to allow the processor to generate a STOP condition. When ports P3 to P7 are used as inputs, they must be programmed to their high-impedance state.

The POR flag (Power-On Reset) is set to 1 at power-on and when V_{CC} goes below 3 V. The flag is reset when an end of data is detected by the TSA5055T (end of a READ sequence). Control of the loop is made possible with the in-lock flag FL, which indicates when the loop is phase-locked (FL = 1).

Table 2 Read data format (see notes 1 to 5)

BYTE	MSB	DATA BYTE						LSB	COMMAND	
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	–	byte 2

Notes

1. POR: Power-on reset flag (POR = 1 on power-on).
2. FL: in-lock flag (FL = 1 when the loop is phase-locked).
3. I2, I1 and I0: digital information for I/O ports P7, P5 and P4 respectively.
4. A2, A1 and A0: digital outputs of the 5-level ADC. Accuracy is ½ LSB (see Table 4).
5. MSB is transmitted first.

Bits I2, I1 and I0 represent the status of the I/O ports P7, P5 and P4, respectively. A logic ‘0’ indicates a LOW level and a logic ‘1’ a HIGH level (TTL levels). A built-in 5-level ADC is available at I/O port P6. This ADC can be used to feed AFC information to the controller from the IF section of the receiver, as shown in Fig.4. The relationship between bits A2, A1, A0 and the input voltage at port P6 is given in Table 4.

Table 3 Address selection

MA1	MA0	VOLTAGE APPLIED ON PORT P3
0	0	0 to $0.1V_{CC}$
0	1	always valid
1	0	$0.4V_{CC}$ to $0.6V_{CC}$
1	1	$0.9V_{CC}$ to 13.5 V

Address selection; see Table 3

The module address contains programmable address bits (MA1 and MA0), which offer the possibility of having several synthesizers (up to three) in one system. The relationship between MA1 and MA0 and the input voltage at port P3 is given in Table 3.

Table 4 ADC levels

A2	A1	A0	VOLTAGE APPLIED ON PORT P6
1	0	0	$0.6V_{CC}$ to V_{CC}
0	1	1	$0.45V_{CC}$ to $0.6V_{CC}$
0	1	0	$0.3V_{CC}$ to $0.45V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.3V_{CC}$
0	0	0	0 to $0.15V_{CC}$

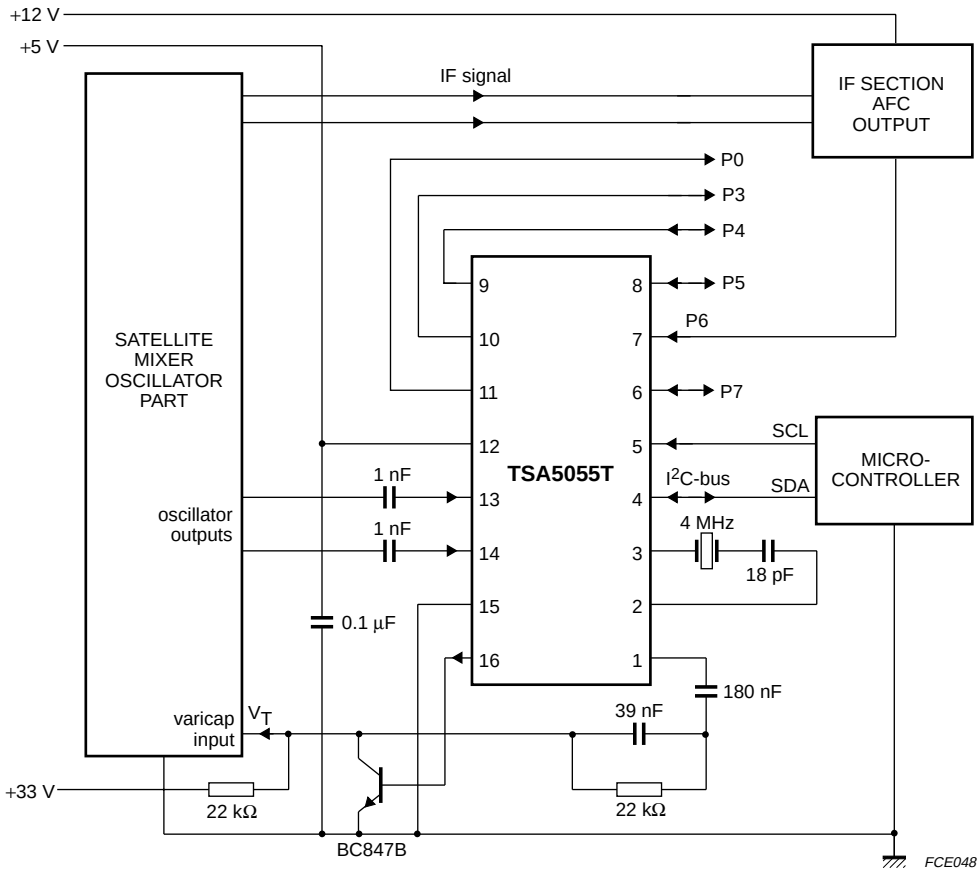


Fig.3 Symmetrical application diagram.

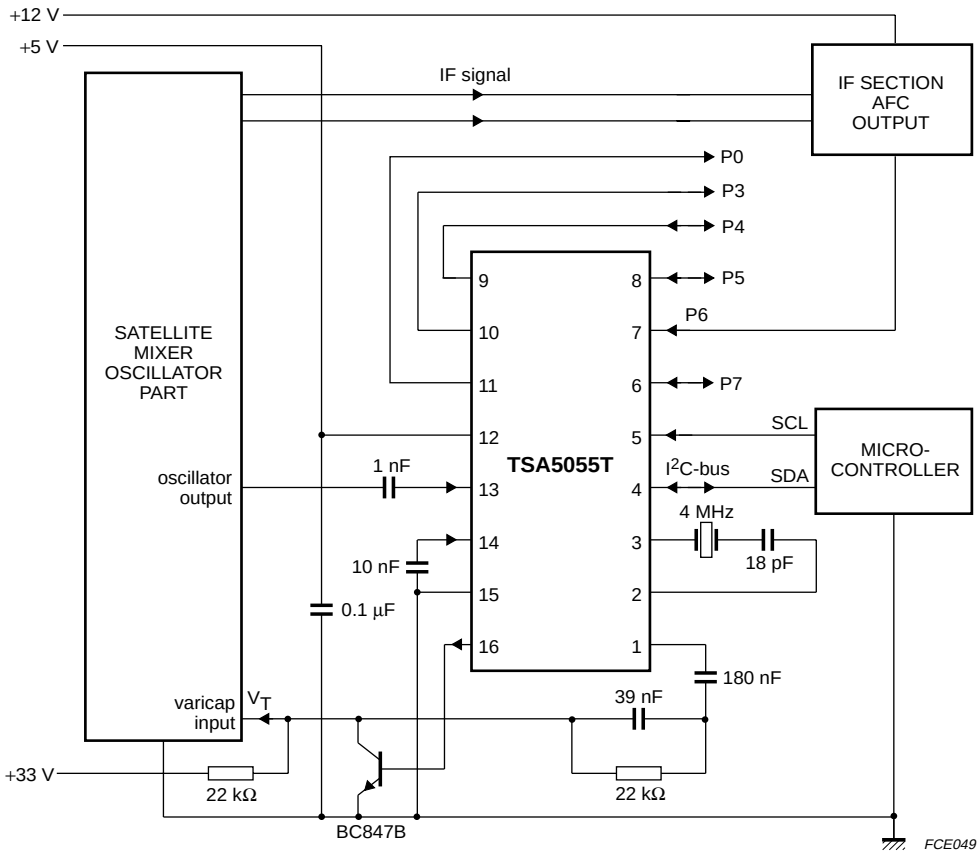


Fig.4 Asymmetrical application diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	+6	V
$V_{O(PD)}$	charge-pump (PD) output voltage	–0.3	V_{CC}	V
$V_{I(Q1)}$	crystal (Q1) input voltage	–0.3	V_{CC}	V
$V_{I/O(SDA)}$	serial data (SDA) input/output voltage	–0.3	+6	V
$V_{I(SCL)}$	serial clock (SCL) input voltage	–0.3	+6	V
$V_{I/O(P7-P0)}$	input/output ports (P7 to P3 and P0) voltage	–0.3	+16	V
$V_{I(RFIN)}$	prescaler inputs (RF_{IN1} and RF_{IN2}) voltage	–0.3	+2.5	V
$V_{O(UD)}$	drive output (UD) voltage	–0.3	V_{CC}	V
$I_{O(P4-P7)}$	output ports (P7 to P4) current (open-collector)	–1	+15	mA
$I_{O(SDA)}$	serial data (SDA) output current (open-collector)	–1	+5	mA
T_{stg}	storage temperature	–40	+150	°C
T_j	maximum junction temperature	–	150	°C

HANDLING

All pins withstand the ESD test in accordance with *"MIL-STD-883C"*, category A (1000 V).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	from junction to ambient	in free air	110	K/W

CHARACTERISTICS

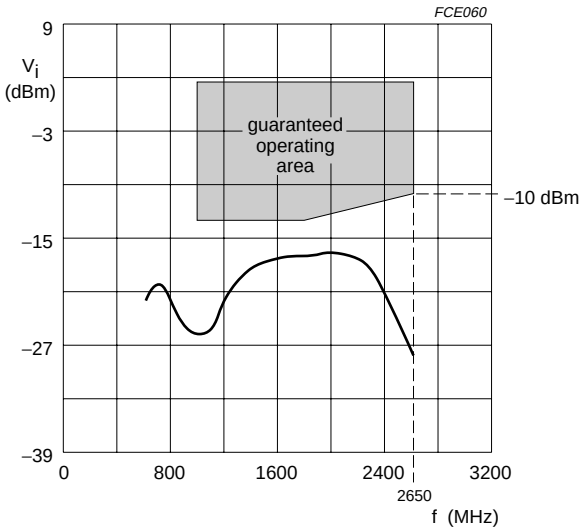
V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage range		4.5	5	5.5	V
T_{amb}	ambient temperature		–20	–	+85	°C
f_{RF}	RF input frequency range		1	–	2.65	GHz
N	divider ratio		256	–	32767	
I_{CC}	supply current		–	60	80	mA
f_{XTAL}	crystal oscillator frequency		3.2	4	4.48	MHz
Z_{XTAL}	crystal oscillator impedance (pin 2)	absolute value	600	1000	–	Ω
$V_{XTAL(p-p)}$	drive level on pin 2 (quartz Philips 4322 143 04093) (peak-to-peak value)		–	110	–	mV
$V_{I(rms)}$	input voltage level (RMS value) f = 1 to 1.8 GHz f = 1.8 to 2.65 GHz	V_{CC} = 4.5 to 5.5 V; T_{amb} = –20 to +85 °C; see typical sensitivity curve in Fig.5	 50/–13 70/–10	 – –	 300/2.6 300/2.6	 mV/dBm mV/dBm
R_I	prescaler input impedance	see Smith chart in Fig.6	–	50	–	Ω
C_I	input capacitance		–	2	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output ports P3 and P0 (current limited)						
I_{LO}	leakage current	V_o = 13.5 V	–	–	10	µA
I_{OS}	output sink current	V_o = 13.5 V	0.7	1	1.5	mA
Output ports P7 to P4 (open collector); see note 1						
I_{LO}	leakage current	V_o = 13.5 V	–	–	10	µA
V_{OL}	output voltage LOW	I_o = 10 mA; note 2	–	–	0.7	V
Input ports P6 and P3						
I_{IH}	input current HIGH	V_{IH} = 13.5 V	–	–	10	µA
I_{IL}	input current LOW	V_{IL} = 0 V	–10	–	–	µA
Input ports P7, P5 and P4						
V_{IH}	input voltage HIGH		2.7	–	–	V
V_{IL}	input voltage LOW		–	–	0.8	V
I_{IH}	input current HIGH	V_{IH} = 13.5 V	–	–	10	µA
I_{IL}	input current LOW	V_{IL} = 0 V	–10	–	–	µA
Bus inputs SCL and SDA						
V_{IH}	input voltage HIGH		3	–	5.5	V
V_{IL}	input voltage LOW		–	–	1.5	V
I_{IH}	input current HIGH	V_{IH} = 5 V; V_{CC} = 0 V	–	–	10	µA
		V_{IH} = 5 V; V_{CC} = 5 V	–	–	10	µA
I_{IL}	input current LOW	V_{IL} = 0 V; V_{CC} = 0 V	–10	–	–	µA
		V_{IL} = 0 V; V_{CC} = 5 V	–10	–	–	µA
Output SDA (open-collector)						
I_{OH}	leakage current	V_{OH} = 5.5 V	–	–	10	µA
V_{OL}	output voltage	I_{OL} = 3 mA	–	–	0.4	V
Charge-pump output PD						
I_{OH}	output current HIGH (absolute value)	CP = 1	90	220	300	µA
I_{OL}	output current LOW (absolute value)	CP = 0	22	50	75	µA
V_O	output voltage	in-lock	1.5	–	2.5	V
$I_{O(leak)}$	off-state leakage current	T0 = 1	–5	–	+5	nA
Operational amplifier output UD (test mode: T0 = 1)						
V_O	output voltage	$V_{O(PD)}$ = 0 V	–	–	100	mV
	output voltage when switched off	T0 = 1; OS = 1; $V_{O(PD)}$ = 2 V	–	–	250	mV
h_{FE}	operational amplifier current gain $\frac{I_{O(UD)}}{I_{O(PD)} - I_{O(PD\ leak)}}$	T0 = 1, OS = 0; $V_{O(PD)}$ = 2 V $I_{O(UD)}$ = 10 µA	2000	–	–	

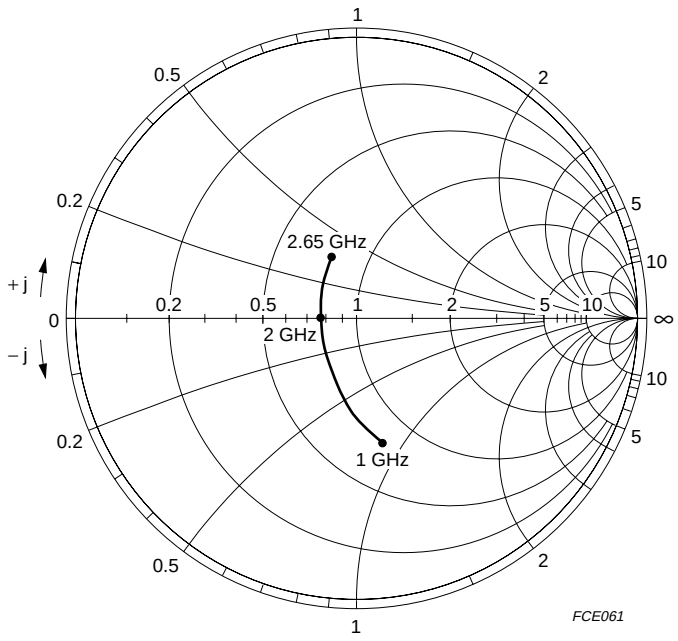
Notes

1. When a port is active, the collector voltage must not exceed 6 V.
2. Measured with a single open-collector active.



V_{CC} = 5 V; T_{amb} = 25 °C.

Fig.5 Typical input sensitivity curve.



V_{CC} = 5 V; reference value = 50 Ω.

Fig.6 Smith chart of typical input impedance.

FLOCK FLAG DEFINITION (FL)

When the FL flag is 1, the maximum frequency deviation (Δf) from stable frequency can be expressed as follows:

$$\Delta f = \pm\left(\frac{K_{VCO}}{K_O} \times I_{CP} \times \frac{C1 + C2}{C1 \times C2}\right)$$

where:

K_{VCO} = oscillator slope (Hz/V)

I_{CP} = charge-pump current (A)

$K_O = 4 \times 10^6$

C1 and C2 = loop filter capacitors.

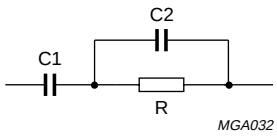


Fig.7 Loop filter.

Flock flag settings

PARAMETER	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	µs
Time span between the loop losing lock and FL-flag resetting	0	128	µs

Flock flag application

- K_{VCO} = 50 MHz/V
- I_{CP} = 220 µA
- C1 = 180 nF
- C2 = 39 nF
- $\Delta f = \pm 85.8$ kHz.

EQUIVALENT INPUT CIRCUITS

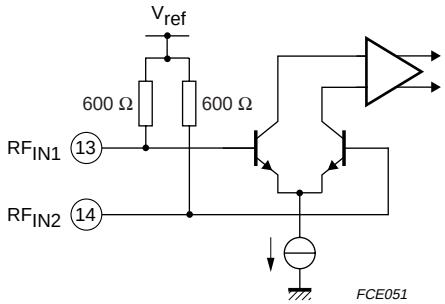


Fig.8 RF input amplifier.

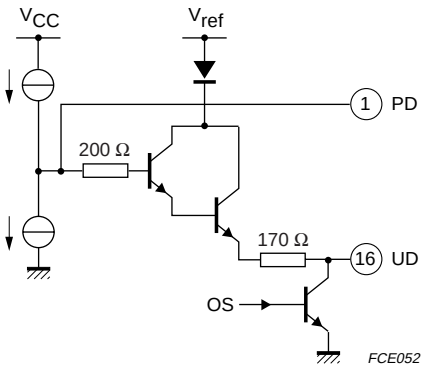
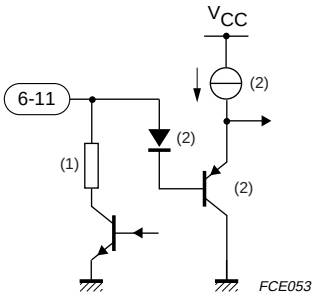


Fig.9 Current amplifier.



(1) This resistor is implemented only for P0 and P3.
(2) These components are not implemented for P0.

Fig.10 Input/output ports, pins 6 to 11.

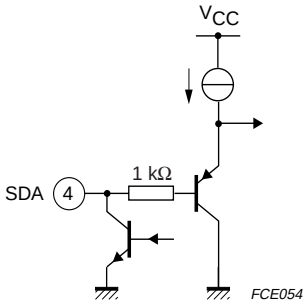


Fig.11 I²C SDA.

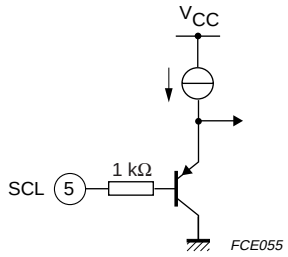


Fig.12 I²C SCL.

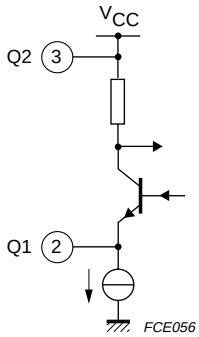
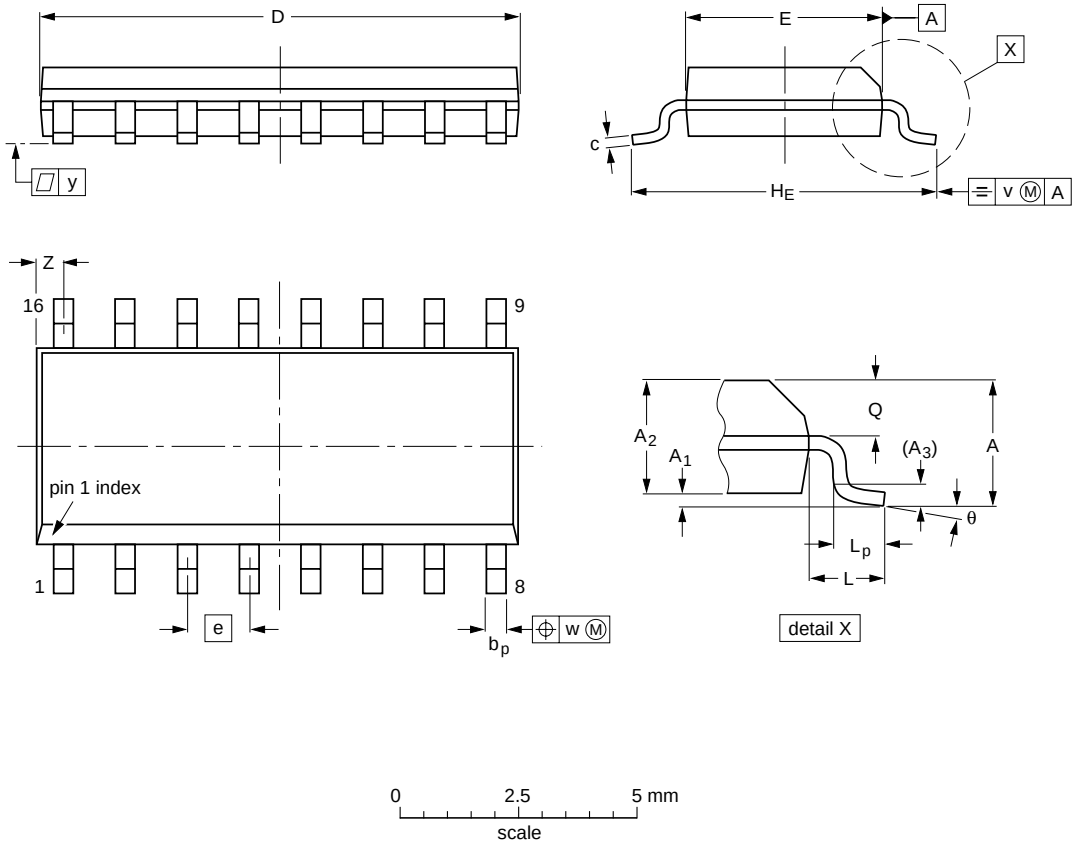


Fig.13 Reference oscillator.

PACKAGE OUTLINE

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 62 5344, Fax.+381 11 63 5777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

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